

### REMARKS

Claims 1-28 have been cancelled without prejudice. Claims 29-42 have been added. Reconsideration in view of the amendments and remarks is hereby requested.

Examiner has objected to the drawings, stating that "Therefore, the 'Display manager' (claims 1, 15); 'the display manager is connected to the image buffers' (claim 16); the system comprising a decoder and first and second processors (claims 1, 2, and 4) must be shown or the feature(s) canceled from the claim(s)." Office Action, at 2. Applicants have canceled all of the indicated claims and respectfully submit that the drawings show every feature of the pending claims, claims 29-44.

Examiner rejected claims 2-14, 18-23, and 25-28 under 35 U.S.C. § 112, 1<sup>st</sup> Paragraph. Applicants have canceled each of the foregoing claims, but respectfully traverse Examiner's contention that "The specification fails to teach or describe the claimed 'the first memory stores a first set of instructions' (Claims 11, 21); 'second memory stores a second set of instructions' (claim 14)". Office Action, at 3. Applicants submit that the application teaches the foregoing. For example, Applicants call Examiner's attention to paragraphs 42 ("The second processor 307 executes code that is also stored in the DRAM 309") and 43 ("The first processor 305 may run code that may be stored in the SRAM 303").

Claims 1, 15-17, and 24 were rejected in view of Jiang. The foregoing claims have been canceled without prejudice and claims 29-42 have been added. Claim 29 is directed to "a system for displaying images, said systems comprising: a first processor for decoding the images in a

decoding order; and a second processor for determining a display order for the images, wherein the display order is different from the decoding order; and wherein the first processor prepares the decoded images for display in the display order determined by the second processor."

\* Claim 39 claims "A circuit for displaying images, said circuit comprising: a processor; and a memory connected to the processor, said memory storing a plurality of instructions that are executable by the processor, wherein execution of the instructions by the processor causes: decoding the images in a decoding order; receiving an indication from another processor, said indication indicating a display image in a display order, wherein the display order is different from the decoding order; and preparing the display image for display."

Applicants respectfully submit that Jiang does not teach the foregoing. Examiner has indicated that Jiang "teaches a system (Fig. 1) for displaying images on a display (150) comprising a decoder (180) for decoding images and parameters associated with the images; ... a display engine (226) for receiving the decoder parameters and displaying the decoded images based on the decoded parameters." Office Action, at 4-5 (Emphasis Added).

Thus, Jiang does not teach or fairly suggest, as claimed in claim 29, "a first processor for decoding the images in a decoding order; ... and wherein the first processor prepares the decoded images for display in the display order determined by the second processor." (Emphasis Added). Therefore, for at least the foregoing reason, claim 29 is allowable.

Additionally, Jiang does not teach or fairly suggest as claimed in claim 39, that "execution of the instructions by the processor causes: decoding the images in a decoding order; ... and preparing the display image for display."


Accordingly, for at least the foregoing reasons, Applicants respectfully submit that claims 29 and 39, and dependent claims 30-38, and 40-42 are allowable.

### Conclusion

In view of the foregoing remarks and amendments each of the pending claims are allowable. Applicants respectfully submit that the Application now stands in a condition for allowance, and the Examiner is requested to pass this case to issuance.

RESPECTFULLY SUBMITTED,

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